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Research Article

Design of an All-Digital Synchronized Frequency Multiplier Based on a Dual-Loop (D/FLL) Architecture

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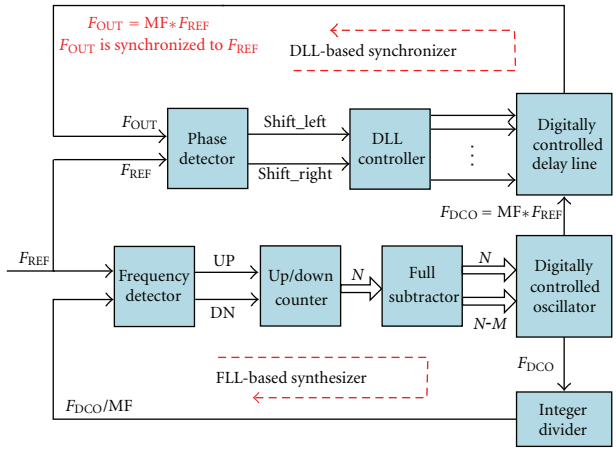
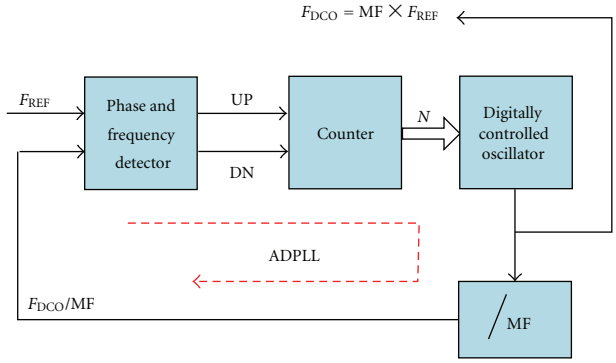
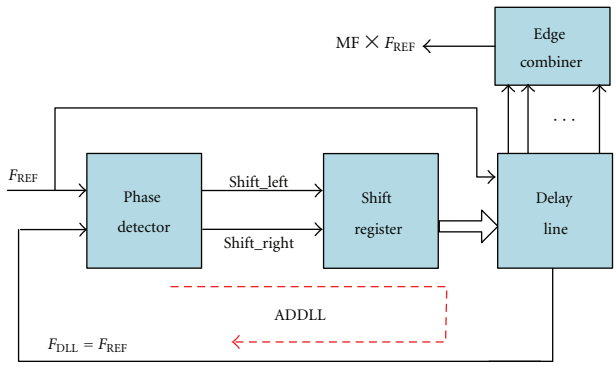
This paper presents a new architecture for a synchronized frequency multiplier circuit. The proposed architecture is an all-digital dual-loop delay- and frequency-locked loops circuit, which has several advantages, namely, it does not have the jitter accumulation issue that is normally encountered in PLL and can be adapted easily for different FPGA families as well as implemented as an integrated circuit. Moreover, it can be used in supplying a clock reference for distributed digital processing systems as well as intra/interchip communication in system-on-chip (SoC). The proposed architecture is designed using the Verilog language and synthesized for the Altera DE2-70 development board. The experimental results validate the expected phase tracking as well as the synthesizing properties. For the measurement and validation purpose, an input reference signal in the range of 1.94–2.62 MHz was injected; the generated clock signal has a higher frequency, and it is in the range of 124.2–167.9 MHz with a frequency step (i.e., resolution) of 0.168 MHz. The synthesized design requires 330 logic elements using the above Altera board.

1. Introduction

Over the years, the phase-locked loops (PLLs) and delay-locked loops (DLLs) are widely employed in the data communication systems including, but not limited to, the implementation of the frequency multiplication and clock synchronization circuits [1, 2]. However, due to the rapid advances in integrated circuit (IC) fabrication technology and the progress in improving the overall system performance, all-digital implementations of such PLLs/DLLs have become more attractive. The all-digital implementations offer the possibility to achieve a low-voltage operation, low-power consumption, and less sensitivity to the noise [3].

Unfortunately, given an identical noise environment and circuit components, the PLL has higher jitter than the DLL due to phase noise accumulation process [4]. Consequently, several all-digital implementations of the PLL have been proposed to enhance the jitter performance. The implementations could be roughly categorized into two types. The first type is an all-digital cell-based architecture [3] where two digitally controlled oscillators (DCOs) are used to effectively decrease the clock jitter. The inner DCO is used for closing the loop and tracking the reference clock, while the outer DCO is used for generating the output clock based on averaging the output of the inner DCO's controller. However, the power consumption and chip area are greatly increased. The second type [5] utilizes a time-to-digital converter (TDC) as a digital filter to increase the resolution of the phase error measurement and hence decrease the jitter performance. Meanwhile, all-digital implementations of DLLs suffer as well from two major drawbacks. First, the multiplication ratio of the reference clock signal depends mainly on the number of delay cells in the delay line. Second, any mismatch in the edge combining logic will be translated directly into a duty-cycle error and fixed-pattern jitter [4]. The aforesaid approaches of enhancing the jitter performance of the PLLs/DLLs have significantly necessitated performing more analytical studies to analyze the performance of the PLLs, DLLs, and dual-loop-based frequency multiplier architectures in a comparable environment. For instance, the analytical studies in [4, 6] show that while the DLL-based frequency multiplier outperforms

Table 1: All-digital frequency multiplier architectures comparison.

Proposed D/FLL architecture

Advantages (i) No phase error accumulation. (ii) The multiplication factor is controllable. (iii) Portable. Disadvantages (i) Dual-loop architecture.
ADPLL [3, 5]

Advantages (i) Single-loop architecture. (ii) Able to achieve wide lock range. Disadvantages (i) Phase error accumulation. (ii) Frequency fine tuning mechanism is challenging.
ADDLL [2, 4]

Advantages (i) Single-loop architecture. (ii) No phase error accumulation. Disadvantages (i) Limited phase capturing range. (ii) The multiplication factor is not controllable. (iii) Edge combining circuit is needed. (iv) Any mismatch in the edge combining logic will be translated directly into a duty-cycle error and fixed-pattern jitter.

the PLL based in term of rejecting the on-chip noise, the latter is better suited for rejecting the noise of the input reference clock. According to relatively recent studies in [7–10], the dual-loop architectures have shown a potential in attenuating both the on-chip and input clock noise, and they do not have the accumulated jitter issue. The current state-of-the-art dual-loop architectures are analog since they include voltage controlled oscillator (VCO) and analog loop filter. In this work, we proposed a fully digital wide-range synchronized frequency multiplier with a high multiplication factor. The implemented architecture requires no analog components and can be easily adapted for different FPGA families as well as implemented as an integrated circuit.

The rest of the paper is organized as follows. Section 2 shows the proposed architecture, and Section 3 describes the building blocks. Section 4 shows the experimental results, and Section 5 gives the conclusions.

2. Operation Overview

This section describes the schematic of the overall architecture for the proposed all-digital dual-loop D/FLL circuit. As shown in Table 1, the D/FLL circuit is composed of proposed frequency-locked (FLL) and delay-locked (DLL) loops that share a common reference clock signal (F_{REF}). In the FLL feedback path, the frequency locking starts from the middle frequency band of the DCO. The output clock signal of the DCO (F_{DCO}) is then scaled down by an integer divider and connected to the frequency detector. The integer divider allows the divided output clock (F_{DCO}/MF) to be relatively convergent with the frequency of F_{REF}. It provides also the ability to select an integer multiplication factor (MF) of the F_{REF} signal frequency (e.g., MF = 2, 4, 8, 16, 32, or 64).

The frequency detector (FD) detects the frequency difference between the F_{REF} and the F_{DCO}/MF signals. The FD then generates an up (UP) or down (DN) signal to indicate that the DCO should be speeded up or slowed down, respectively. Then, both up/down counter and full subtractor update the DCO control word to adjust the output frequency of the DCO. Meanwhile, the phase detector (PD) provides a phase locking between the F_{DCO} and the F_{REF} signals. It

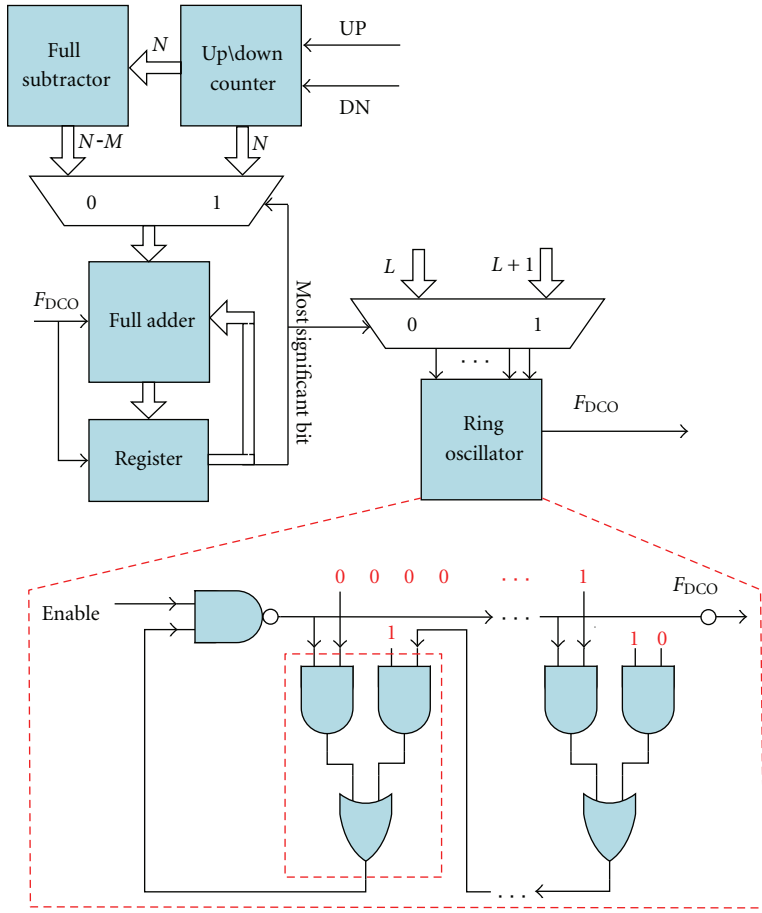


Figure 1: Functional block diagram of the digitally controlled oscillator.

then generates a shift right (shift_right) signal or shift left (shift_left) signal to adjust the delay of the digitally controlled delay line. The D/FLL circuit will generate an output signal (F_{OUT}) that is synchronized with respect to the F_{REF} signal as well as MF times the F_{REF} frequency.

The advantages of the proposed all-digital dual-loop D/FLL architecture are listed and compared to the existing state-of-the-art architectures, as shown in Table 1. The proposed architecture simultaneously generates a high frequency signal from a low frequency reference signal and synchronizes the two signals without the jitter accumulation issue of PLL-based implementation. Moreover, the proposed architecture is portable and can be easily implemented as an integrated circuit. The simultaneous dual properties enhance the stability of the system and can be used in supplying a clock reference for distributed digital processing systems as well as intra/interchip communication in system-on-chip (SoC) [11].

3. Circuit Design and Implementation

The basic operation of the D/FLL circuit requires seven important building blocks to provide frequency and phase locking.

3.1. Digitally Controlled Oscillator (DCO). A digitally controlled oscillator previously proposed in [12] is used in the proposed FLL design that has the ability to generate multiples of the F_{REF} signal frequency. It consists of two main blocks: ring oscillator and fractional divider, as shown in Figure 1. The ring oscillator consists of one NAND gate which enables/disables the oscillation and a chain of AND-OR delay elements. The ring oscillator produces a clock signal (F_{OSC}) whose frequency is proportional to the number of the delay elements in the ring. The F_{OSC} is given by

$$F_{OSC} = \frac{1}{2Lt_{de}}, \tag{1}$$

where t_{de} is the time delay for each delay element and L is the chain length that is defined by a one-hot coded control word. The F_{OSC} signal must go through each of the delay elements twice to provide one period of oscillation. Consequently, reducing the number of the delay elements in the ring gives higher frequency and vice versa. Moreover, changing the ring oscillator chain length via a one-hot coded word provides a coarse frequency resolution as shown experimentally in Figure 2. The fractional divider comprises an adder-accumulator. The most significant bit of the accumulator signed register is used to switch the input of the adder

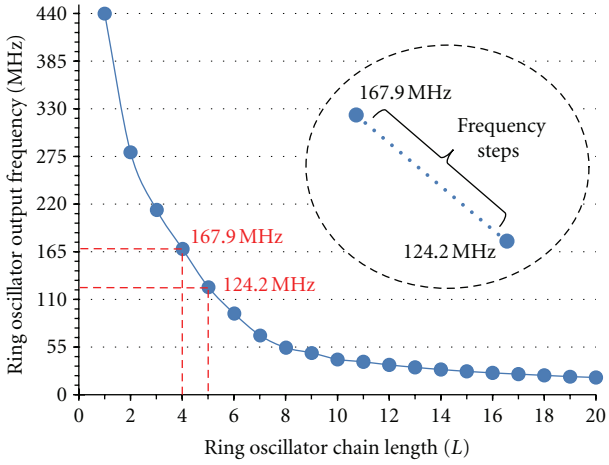


Figure 2: Measured ring oscillator output frequency F_{OSC} versus chain length. The number of bits of N defines the number of frequency steps between the two extreme limits (167.9 and 124.2 MHz).

between signed integer number N and its two's complement N-M. It is also used to switch between two adjacent ring oscillator chain lengths, ($L1$) and ($L2$).

The digitally controlled oscillator output clock frequency F_{DCO} is given by

$$F_{DCO} = \frac{M}{(N/(F_{OSC}(L1))) + ((M\text{-}N)/(F_{OSC}(L2)))}. \quad (2)$$

Accordingly, switching between two adjacent chain lengths $L1$ and $L2$ provides on average fine frequency resolution. Typically, the DCO must be able to provide a high frequency resolution as well as very good frequency stability.

Good frequency stability is normally achieved by designing a stable and fast controller to control the DCO, whereas a high frequency resolution is achieved by increasing the number of bits of the accumulator signed register.

3.2. Integer Divider. The integer divider consists of a chain of divide-by-2 circuits. Each circuit is a single D flip-flop. The presence of the integer divider block in the frequency locked loop is to scale down the output clock signal of the DCO to be relatively convergent with the frequency of F_{REF} and allows the latter to run at a low frequency. The divider provides also the ability to select an integer multiplication factor (MF) of the F_{REF} signal frequency (e.g., MF = 2, 4, 8, 16, 32, or 64).

3.3. Frequency Detector (FD). The block diagram of the rotational frequency detector is given in [13]. The rotational FD has three inputs, the F_{REF} signal and the in-phased I and the quadrature Q signals of the F_{DCO}/MF signal. As shown in Figure 3, I and Q signals are sampled by the transitions of the reference clock at the four D flip-flops. The DFF1 and DFF2 store the current sampled output, whereas DFF3 and DFF4 store the previous sampled output. Thus, the frequency difference is detected, and UP and DN signals are generated using two AND gates. The frequency of UP or DN signal is

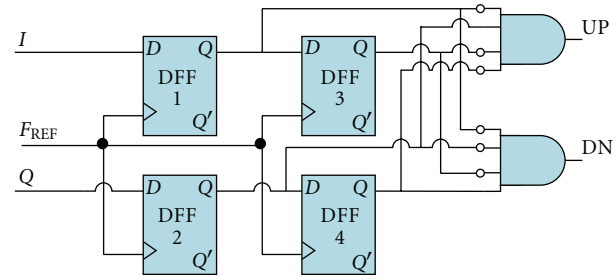


Figure 3: Block diagram of the rotational frequency detector.

equal to the difference between the frequency of I and the reference clock frequency.

The rotational frequency detector becomes ineffective when the frequency of I exceeds 30% of the reference clock frequency. However, the integer divider in the frequency locked loop scales down the frequency of I to be relatively convergent with the frequency of F_{REF}. As a result, the integer divider scales down the difference in frequencies to less than 30%.

3.4. Up/Down Counter and Full Subtractor. The up/down counter and full subtractor are used to generate the signed integer number N and its two's complement N-M, respectively. First of all, the counter used is a normal nine-bit synchronous up/down counter. It has two input signals, Up/$\overline{\text{Down}}$ and clk. However, the Up/$\overline{\text{Down}}$ and clk signals are formulated by

$$\begin{aligned} \text{Up}/\overline{\text{Down}} &= \text{UP} + \overline{\text{DN}}, \\ \text{clk} &= \left((\text{UP} + \text{DN}) \cdot \left(\overline{\text{UP}} + \overline{\text{DN}}\right)\right) \cdot F_{REF}. \end{aligned} \quad (3)$$

Based on the received UP or DN signal from the FD, the up/down counter generates nine bits output signal N, which is required for the DCO operations. For each decision, the counter updates N value by adding or removing one from the current N value. Second of all, the subtractor used is also a normal nine-bit full subtractor. It generates nine bits output signal (N-M) based on N and M values, where all bits of M value are set to be 1.

3.5. Digitally Controlled Delay Line (DCDL). In this work, the phase tracking mechanism is separated from the frequency tracking loop. This approach adds an essential benefit to the design which is the ability to synchronize the output clock signal with the input reference signal. The success of the phase locking process is based on the presence of a linear relationship between the DLL controller output and the DCDL output delay; thus, a chain of linear delay elements (DE) is employed in the structure of the DCDL [14]. Each DE consists of three NAND gates. One of them is used to activate the selected DE, while the other two gates are used to delay/advance the F_{DCO} signal. An additional NAND gate is added to the delay line chain to produce the original signal without inversion.

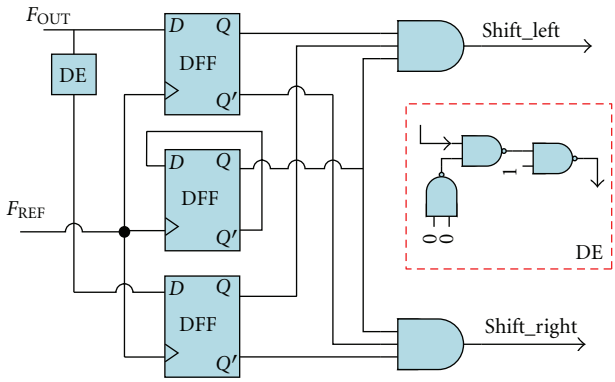


Figure 4: Block diagram of the phase detector.

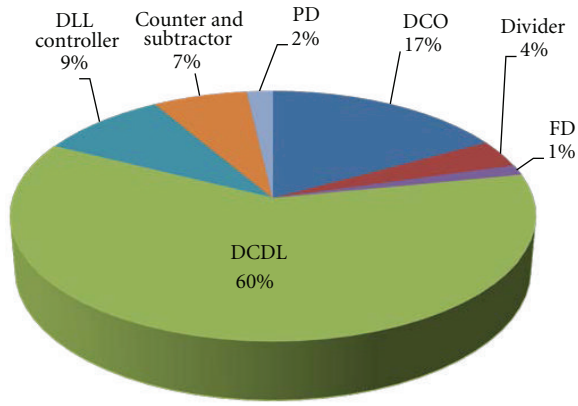


Figure 5: Total number of the logic elements utilization breakdown.

3.6. DLL Controller. Synchronizing two signals without the jitter accumulation issue requires a stable controller. Consequently, a linear controller is used in the phase locking. The DLL controller is responsible for controlling the DCDL chain length based on the received shift right (shift_right) or shift left (shift_left) signal from the phase detector. For each decision, the DLL controller updates the number of the DEs in the chain. A shift_right signal decreases them and thus decreases the delay of the input clock of the DCDL while a shift_left increases them.

3.7. Phase Detector (PD). The phase detector in [14] is used with modifications as shown in Figure 4. It generates shift_right or shift_left regardless of the frequency difference between F_{REF} and F_{OUT}. As a result, a frequency divider block is not needed in the delay locked loop. The delay element of the detector governs the final phase difference and is set to be identical to the DE of the delay line. Generating shift_left or shift_right once every two cycles of the reference clock provides stability for the DLL controller.

4. Experimental Results

The proposed synchronized frequency multiplier is completely realized as a fully digital architecture. It is designed using Verilog-HDL and synthesized using Altera Quartus II Web Edition v11.0 software for Altera DE2-70 development board, with a Cyclone II EP2C35F672C6 FPGA on board. The fact that it is implemented on an FPGA is a confirmation of its all-digital status; hence, it can be implemented on various platforms, such as FPGAs and ICs. The experimental setup consists of the DE2-70 board, the Agilent 16821A logic analyzer, the Tektronix TDS-5104 digital phosphor oscilloscope with TDSJIT3 software, the Tektronix DPO4104B digital phosphor oscilloscope, and the Advantest R3132 spectrum analyzer.

As illustrated in Figure 5, the total size of the proposed architecture is 330 logic elements (LEs), which is less than 1% of the total number of LEs in the board. The configurations of the system variables are as follow: the two ring oscillator lengths $L1$ and $L2$ are set to be fifth and fourth active delay elements, respectively, M and N are set to be nine-bit

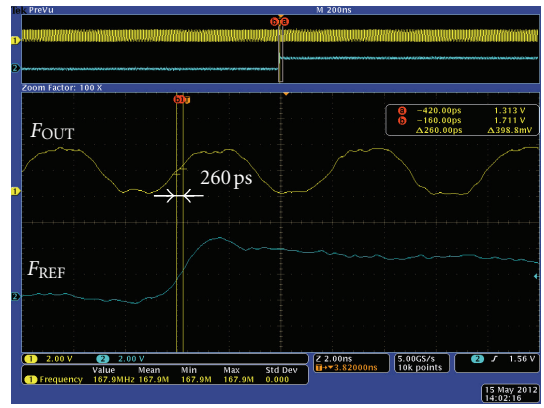


Figure 6: The measured synchronization static phase offset at the locked state (F_{OUT} = 167.9 MHz, F_{REF} = 2.62 MHz).

numbers, whereas M is equal to 255 and N varies from 0 to 255, and the MF is adjusted to be equal to 64. Changing the frequency range of the F_{REF} signal from 1.94 MHz to 2.62 MHz allows the generated F_{OUT} signal to be in the range of 124.2–167.9 MHz with a frequency step (i.e., resolution) of 0.168 MHz.

As illustrated in Figure 6, the F_{OUT} signal is synchronized to the F_{REF} signal with a static phase error equal to 260 ps (less than one DE). As shown in Figure 7, the frequency multiplier requires less than 1.28 ms for both frequency and phase locking. The measured RMS and peak-to-peak jitter of the frequency multiplier are 28.74 and 258.1 ps, respectively, as shown in Figure 8. The measured spectrum of the F_{OUT} signal is shown in Figure 9.

Table 2 presents a performance comparison for the proposed circuit with the previous designs of all-digital frequency multiplier circuits. These circuits were implemented and synthesized for the same technology (Altera DE2-70 development) for a fair comparison. As an overall trend, the proposed architecture has a competitive performance and achieves the highest maximum output frequency compared to the other architectures. Moreover, the proposed

Table 2: Performance comparison for the proposed architecture with existing all-digital designs.

Parameter	Proposed architecture	[15]	[16]
Technology	EP2C35F672C6 Altera-FPGA	EP2C35F672C6 Altera-FPGA	EP2C35F672C6 Altera-FPGA
Area	330 LEs	105 LEs	177 LEs
Power consumption[a] (static, dynamic)	155.02 mW, 4.38 mW	155.59 mW, 7.86 mW	155 mW, 13.31 mW
Measured RMS jitter	28.74 ps	14.82 ps	15.09 ps
Measured peak-to-peak jitter	258.1 ps	333.26 ps	526.49 ps
Maximum output frequency	440 MHz	280 MHz	330 MHz
Frequency resolution	Fine tunning frequency step = 0.168 MHz	Coarse tunning frequency step = 12.47 MHz	Coarse tunning frequency step = 6.25 MHz
Multiplication factor	64	8	16
Portability	Yes	Yes	No
Phase tracking	Yes	No	No

[a] Using Altera PowerPlay power analyzer tool.

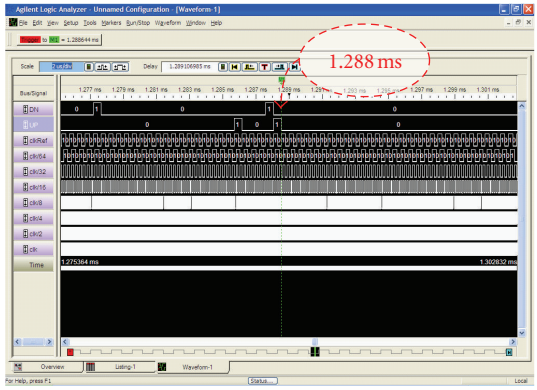


Figure 7: A screenshot for the lock time measurement.

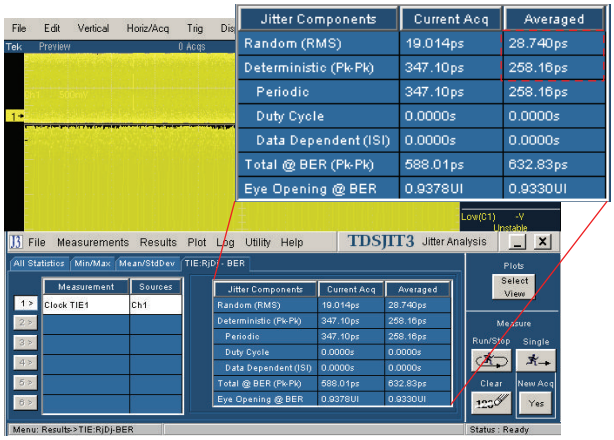


Figure 8: The measured RMS and peak-to-peak jitter (at F_{OUT} = 167.9 MHz).

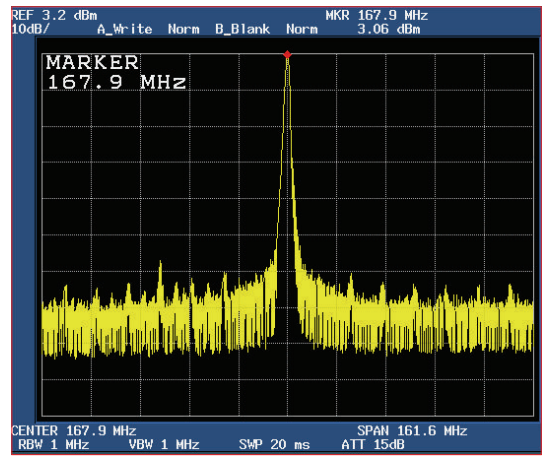


Figure 9: The measured spectrum of the F_{OUT} signal at 167.9 MHz.

5. Conclusions

An all-digital dual-loop (D/FLL) circuit for synchronized frequency multiplier is presented in this paper. The proposed architecture is portable and can be adapted easily for different FPGA families. Moreover, it can be used in supplying a clock reference for distributed digital processing systems as well as intra/interchip communication in system-on-chip (SoC). The experimental results are included, and they validate the expected functionality and properties, such as phase tracking (i.e., synchronization) as well as generating a clean and higher frequency signals from lower frequency signals (i.e., synthesizing). The generated clock frequency is in the range of 124.2–167.9 MHz (it can even be as high as 440 MHz) with a frequency step of 0.168 MHz.

architecture outweighs the existing architectures in providing the highest frequency resolution (smallest frequency steps), better frequency stability, and the highest multiplication factor. However, since the proposed architecture is dual-loop architecture, the occupied number of logic elements is a relatively large compared to the existing architectures.

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